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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,089	12/10/2003	Shinya Sasagawa	740756-2676	6646

22204 7590 10/11/2006

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EXAMINER	
ANGADI, MAKI A	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 10/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,089	SASAGAWA ET AL.	
	Examiner	Art Unit	
	Maki A. Angadi	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 1, 4, 5, 8, 9, 12, 14, 17, 19, 22, 23, 26, 29 and 31 are rejected under 35 U.S.C. 103(a) over Samavedam (US Pub. No. 2004/0023478) in view of Chang (US Patent No. 6,300,196).

As to claims 1, 5, 9, 14, 19 and 23, Samavedam discloses a method of manufacturing a semiconductor device (paragraph 0002) consisting of the steps:

(a) Forming a masking pattern (paragraph 0023) on a laminate consisting of a first conductive layer (110) (Fig.1) and a second conductive layer (114) (paragraph 0025); (b) Forming a first pattern with a tapered sidewall (124, Fig. 4) portion by etching the laminate (paragraph 0031); and (c) Performing a plasma treatment to the first pattern with the tapered sidewall portion (paragraph 0030); and (d) Forming a second pattern by anisotropic etching the first pattern with the tapered sidewall portion (124) (paragraph 0031).

Samavedam discloses the use of metal film that includes, *titanium*, aluminum, zirconium, niobium tantalum and tungsten or an alloy containing any of these elements (paragraph 0022).

Samavedam discloses forming a mask pattern (paragraph 0023) on a laminate consisting of a first conductive layer (110) (Fig.3) and second conductive layer (114) on the first conductive layer (110), and a third conductive layer on the second conductive layer (paragraph 0042).

Samavedam discloses forming a mask pattern on a laminate consisting of a first conductive layer (110) (Fig.3) and a second conductive layer (114) over a semiconductor layer with a gate insulating film (108) interposed there between (paragraph 0030).

Samavedam discloses adding an impurity elements to the semiconductor layer as a shielding mask to form a region with the impurity elements in the semiconductor film wherein the region with the impurity elements overlaps with the first conductive layer (Fig.1, paragraph 0020).

The reference of Samavedam does not expressly disclose the applicants' tapered sidewall (105') (Fig. 1b, c, d). However, Chang discloses the formation of tapered sidewall (118)(Fig.5C, 5F, 5G and 5H) (col.5, lines 62-67, col.6, lines 1-4, col.6, lines 47-49, lines 60-65) using anisotropic etching (col.6, lines 31-36, lines 61-66). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process used by Samavedam to form tapered side wall in the gate structure because Chang illustrates that the generation of tapered side wall by anisotropic etching results in an increased surface area between the dielectric layer and gates which enhances capacitance between the floating gate and the control gate (col.3, lines 60-65).

As to claim 4, 8, 12, 17, 22, 26, and 31, Samavedam discloses that the first conductive layer is made of a metal nitride (paragraph 0030).

As to claim 29, Samavedam discloses that the lower first conductive layer is made of metal nitride (110, Fig.3) (paragraph 0030).

Claim Rejections - 35 USC § 103

2. Claims 2, 3, 6, 7, 10, 11, 13, 15, 16, 18, 20, 21, 24, 25, 27, 28, 30 and 32 are rejected under 35 U.S.C. 103(a) over Samavedam (US Pub. No. 2004/0023478)

in view of Chang (US Patent No. 6,300,196) as applied to claims 1, 5, 14, 19 and 23 in further view of Hori (US Patent No. 5,445,710).

As to claim 2, 6, 10, 15, 20 and 24, Samavedam discloses the plasma treatment using CF_4/Ar or CF_4/HBr or Cl_2 or He chemistry (paragraph 0030) but is silent about the use of pure argon for plasma treatment. However, Hori discloses the use of argon, hydrogen, or fluorocarbon (col.7, lines45-48) and oxygen (col.7, line 54) as an etching gas. Therefore, it would be obvious to one of ordinary skill in the art at the time of invention to use select argon as an etching gas as cited by the applicant in this claim because Hori suggests that the argon as an inert gas is a commonly used carrier gas in plasma deposition (col.7, lines 45-46) and in addition, use of etching gas depends on the material to be processed and etch selectivity desired in any given application (col.10, lines 1-6).

As to claim 3, 7, 11, 16, 21 and 25, Samavedam is silent about plasma treatment to remove polymer residue (paragraph 0030), a reaction product adhering to the tapered sidewall portion is removed by performing the plasma treatment step. However, Hori discloses the use of dry ashing to cause oxygen plasma to remove an organic resist (col.5, lines 13-16). Therefore, it would be obvious to one of ordinary skill in the art at the time of invention to include dry ashing process in the device fabrication discloses by Samavedam because Hori

illustrates that dry ashing process allows the easy removal of resist which cannot be removed by wet etching method (col.5, lines18-21).

As to claim 13, 18, 27 and 32, Samavedam discloses the use of third conductive layer (paragraph 0042) but is silent about the material being used for this process. However, Samavedam discloses the use of high melting point materials such as titanium nitride, iridium, tantalum, rhenium, molybdenum, zirconium for the first and second metal layers (paragraph 0022 and claim 13). Therefore, it would be obvious to one of ordinary skill in the art at the time of invention to use high-melting point material for the third conductive layer because Samavedam teaches that the choice of material for the conductive layer depends on the work function of the metal being close to the valence band of silicon (i.e. a work function of about 5.1 eV) (paragraph 0022).

As to claim 28 and 30, Samavedam discloses a semiconductor device consisting of a gate electrode consisting of a lower first conductive layer and an upper second conductive layer (Fig.4, paragraph 0029) including titanium as its main component (paragraph 0022) and a third conductive layer on the second conductive layer (Fig.3, paragraph 0042).

Samavedam is silent about the width (thickness) of the first, second and third conductive layers (paragraph 0042). The width (thickness) of the conductive layer is dependent on several factors such as, the type of material, etch process

and the doping level desired that could be a result-effective variable that can be optimized. See MPEP § 2144.05 II. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to decide on the thickness of conductive layers so that the width of the first conductive layer is wider than the width of the second and third conductive layers. See MPEP § 2144.05 II.

Response to Arguments

Applicant's arguments with respect to claims 1, 5, 9, 14, 19, and 23 have been considered but are moot in view of the new ground(s) of rejection.

(a) *With respect to independent claims 1, 5, 9, 14, 19 and 23,* applicants' arguments on pages 3-4 that the reference of Samavedam (US Pub No. 2004/0023478) does not expressly disclose the formation of tapered sidewall are convincing. However, a new prior art of Chang (US Patent No. 6,300,196) discloses the formation of tapered sidewall using anisotropic etching in fabricating gate structures (see the arguments on pages 2-4).

(b) *With respect to claim 19,* Samavedam discloses the process of adding n-type impurity (such as phosphorus or arsenic) and p-type impurities (such as boron) in the semiconductor structure (paragraph 0020, lines 25-34).

(c) *With respect claims 20 and 21,* the plasma treatment is clearly discussed in paragraph (0030).

(d) *With respect to claims 28 and 30,* the arguments on pages 6-7 clearly explain the basis for rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nagai (US Pub. No. 2004/0091820) discloses a method for removing a resist pattern and method for manufacturing semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maki A. Angadi whose telephone number is 571-272-8213. The examiner can normally be reached on 8 AM to 4.30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dr.Maki Angadi
Examiner
Art Unit 1765

SHAMIM AHMED
PRIMARY EXAMINER

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :12/19/05, 11/19/04, 10/5/04, 12/10/03.